1. A netlist model of a physical circuit comprising:

a virtual delay element, wherein said virtual delay element is coupled to a circuit element in said physical circuit.

2. A netlist model of a physical circuit as recited in claim 1, wherein an input signal is supplied to the virtual delay element.

3. A netlist model of a physical circuit as recited in claim 2, wherein the input signal is supplied by a test pattern generator.

4. A netlist model of a physical circuit as recited in claim 2, wherein the input signal is supplied by a user.

5. A netlist model of a physical circuit as recited in claim 3, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

6. A netlist model of a physical circuit as recited in claim 4, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

7. A netlist model of a physical circuit as recited in claim 2, wherein the virtual delay element is one of a flip-flop or a latch.

8. A method for generating a model for a physical circuit comprising:

generating a netlist model for said physical circuit; and

providing a virtual delay element to said netlist model, wherein said virtual delay element is coupled to a physical circuit element.

9. A method for generating a model for a physical circuit as recited in claim 8, further comprising providing an input signal for said virtual delay element.

10. A method for generating a model for a physical circuit as recited in claim 9, wherein the input signal is supplied by a test pattern generation system.

11. A method for generating a model for a physical circuit as recited in claim 9, wherein the input signal is supplied by a user.

12. A method for generating a model for a physical circuit as recited in claim 10, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

13. A method for generating a model for a physical circuit as recited in claim 11, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

14. A method for generating a model for a physical circuit as recited in claim 9, wherein the virtual delay element is one of a flip-flop or a latch.

15. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor to implement a method for generating a model for a physical circuit, the method comprising:

generating a netlist model for said physical circuit; and

providing a virtual delay element to said netlist model, wherein said virtual delay element is coupled to an asynchronous circuit element.

16. A set of instructions residing in a storage medium as recited in claim 15, wherein the method for generating a model for a physical circuit further comprises providing an input signal for said virtual delay element.

17. A set of instructions residing in a storage medium as recited in claim 16, wherein the input signal is supplied by a test pattern generation system.

18. A set of instructions residing in a storage medium as recited in claim 17, wherein the input signal is supplied by a user.

19. A set of instructions residing in a storage medium as recited in claim 17, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

20. A set of instructions residing in a storage medium as recited in claim 18, wherein the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

21. A set of instructions residing in a storage medium as recited in claim 16, wherein the virtual delay element is one of a flip-flop or a latch.